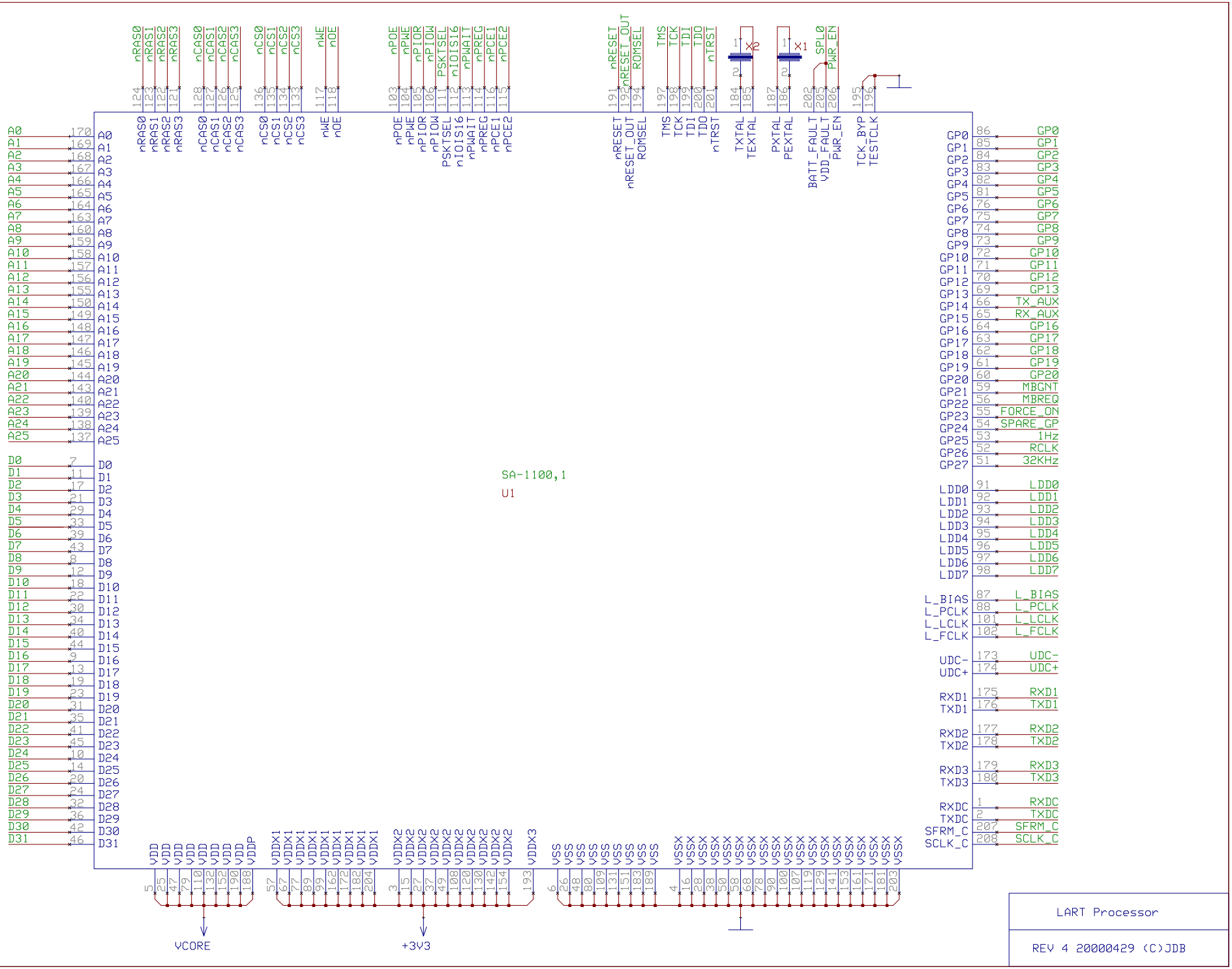
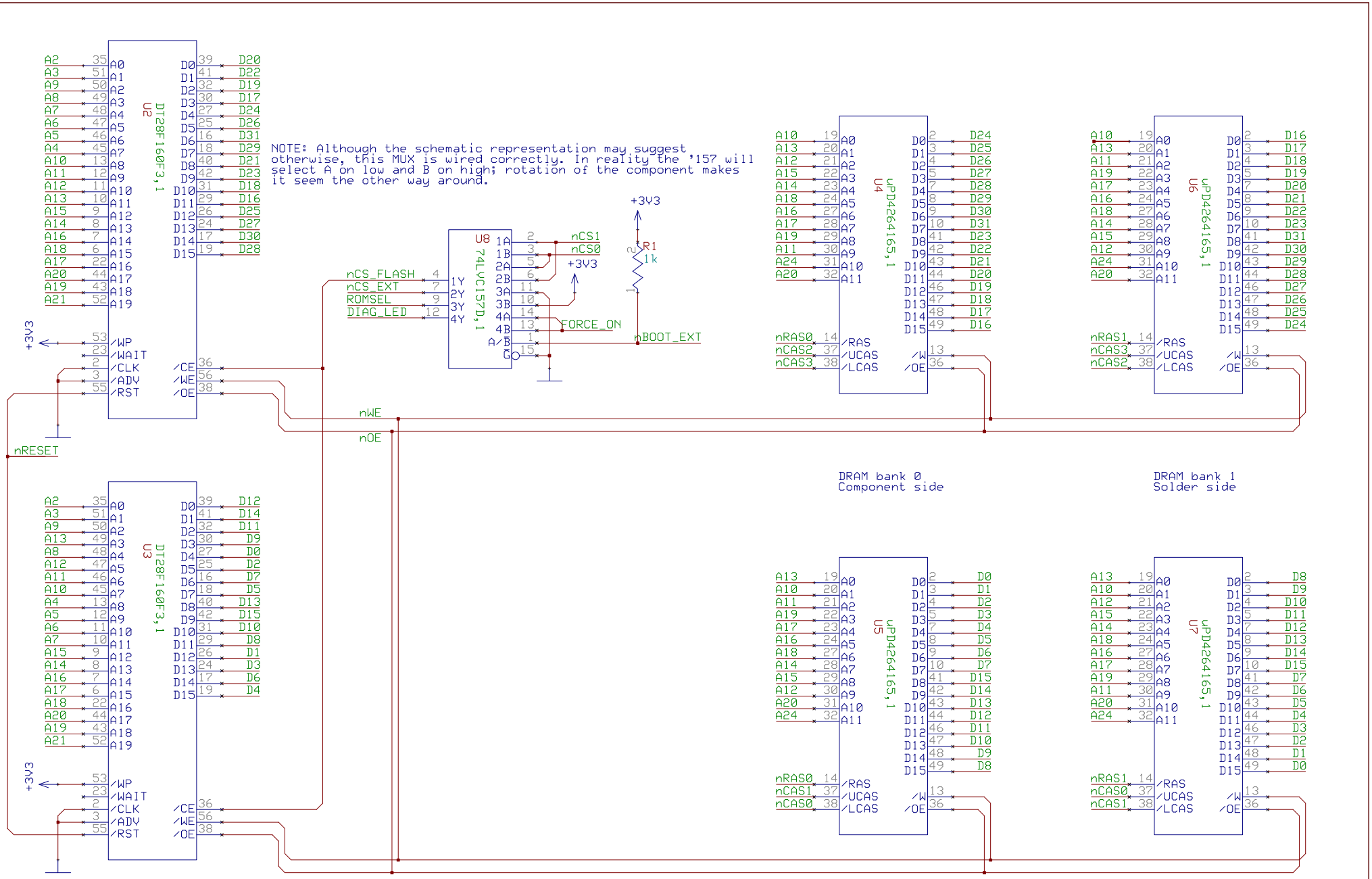

SA-1100,1
U1
nRAS0
nRAS1
nRAS2
nRAS3
nCAS0
nCAS1
nCAS2
nCAS3
nCS0
nCS1
nCS2
nCS3
nWE
nOE
nPOE
nPWE
nPIOR
nPIOW
PSKTSEL
nIOIS16
nPWAIT
nPREG
nPCE1
nPCE2
nRESET
nRESET_OUT
ROMSEL
TMS
TCK
TDI
TDO
nTRST
TXTAL
TEXTAL
PXTAL
PEXTAL
BATT_FAULT
VDD_FAULT
PWR_EN
SPL0
TCK_BYP
TESTCLK
X1
X2
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31
GP0 GP1 GP2 GP3 GP4 GP5 GP6 GP7 GP8 GP9 GP10 GP11 GP12 GP13 TX_AUX RX_AUX GP16 GP17 GP18 GP19 GP20 MBGNT MBREQ FORCE_ON SPARE_GP 1Hz RCLK 32KHz
LDD0 LDD1 LDD2 LDD3 LDD4 LDD5 LDD6 LDD7
L_BIAS L_PCLK L_LCLK L_FCLK
UDC- UDC+
RXD1 TXD1
RXD2 TXD2
RXD3 TXD3
RXDC TXDC SFRM_C SCLK_C
VDD VDDX1 VDDX2 VDDX3 VSS VSSX
VCORE
+3V3
LART Processor
REV 4 20000429 (C)JDB

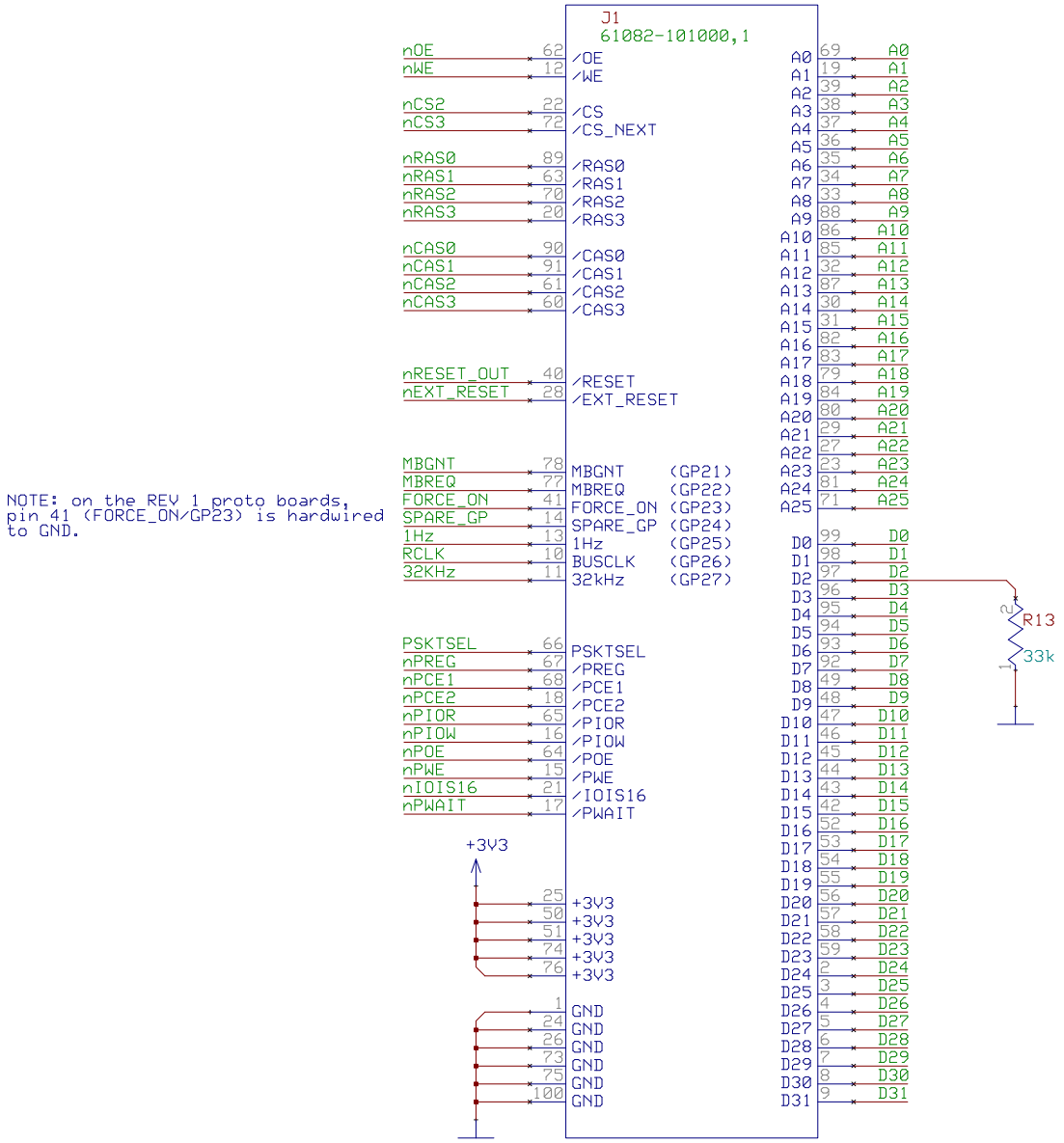


Flash VCC: 1,21,28,33,54
Flash GND: 4,15,20,37
Flash NC : 5,14,34

DRAM VCC: 1,6,12,25
DRAM GND: 26,39,45,50
DRAM NC : 11,15,16,17,18,33,34,35,40

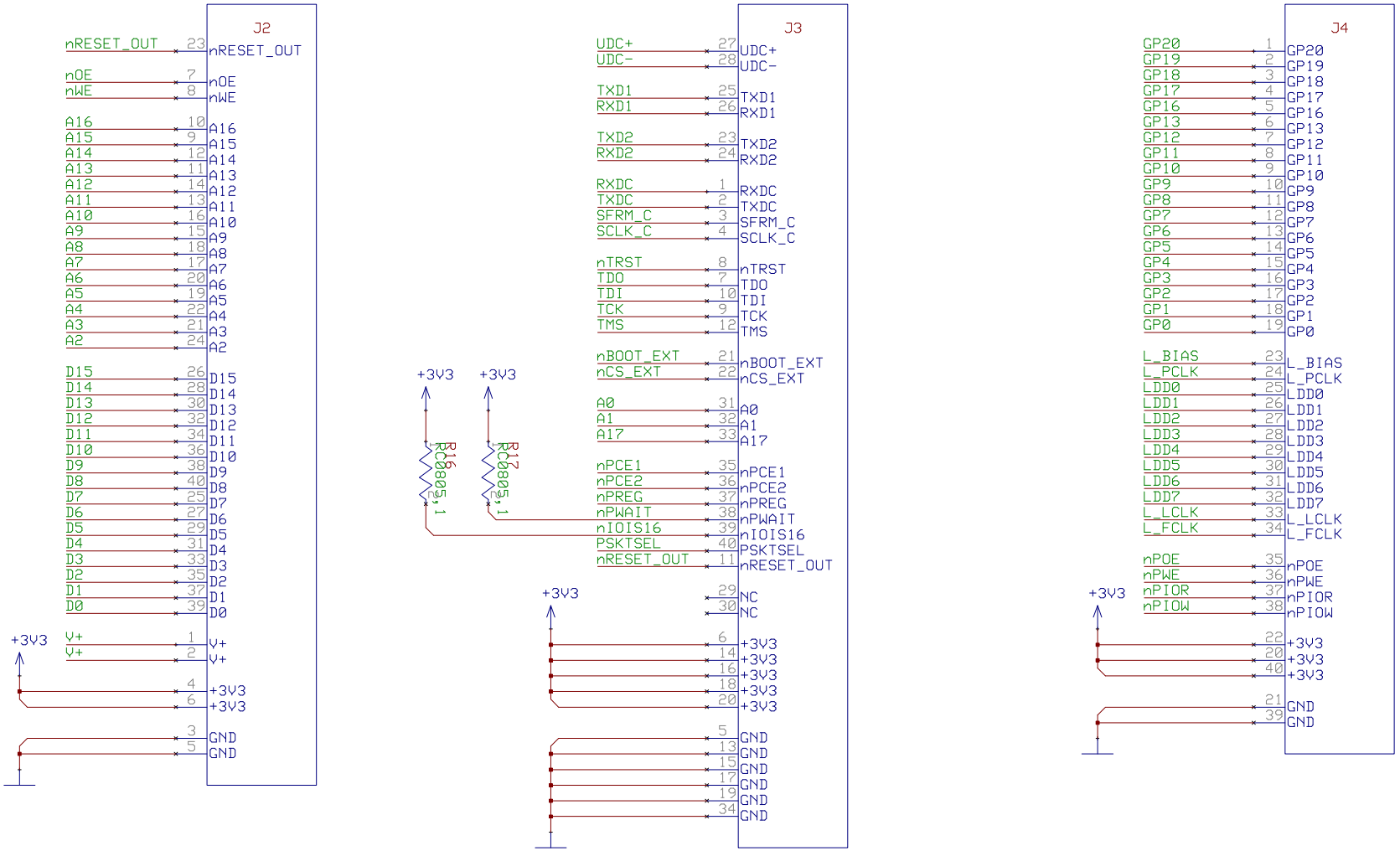
LART Memory

REV 4 20000429 (C)JDB



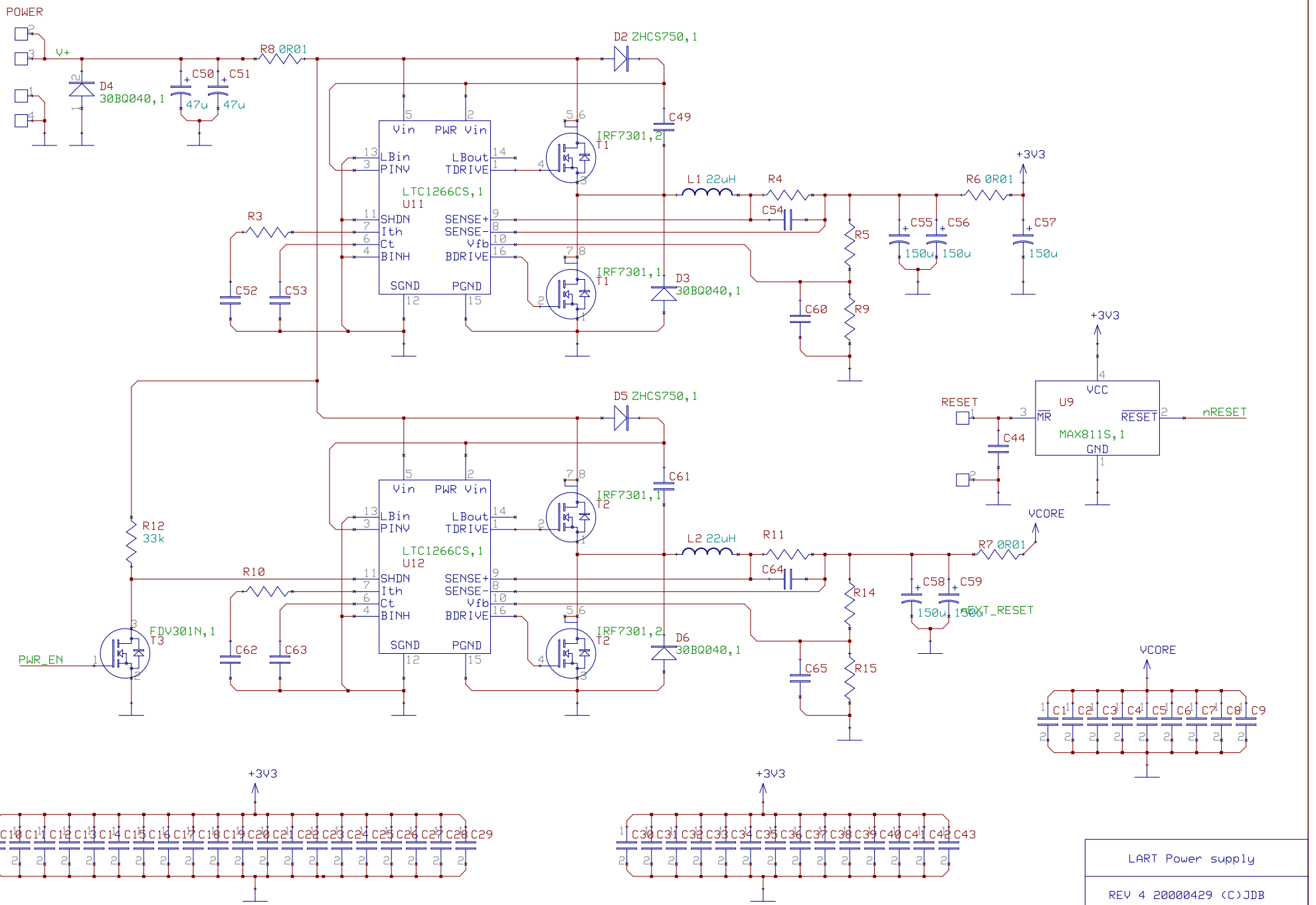
NOTE: on the REV 1 proto boards, pin 41 (FORCE_ON/GP23) is hardwired to GND.

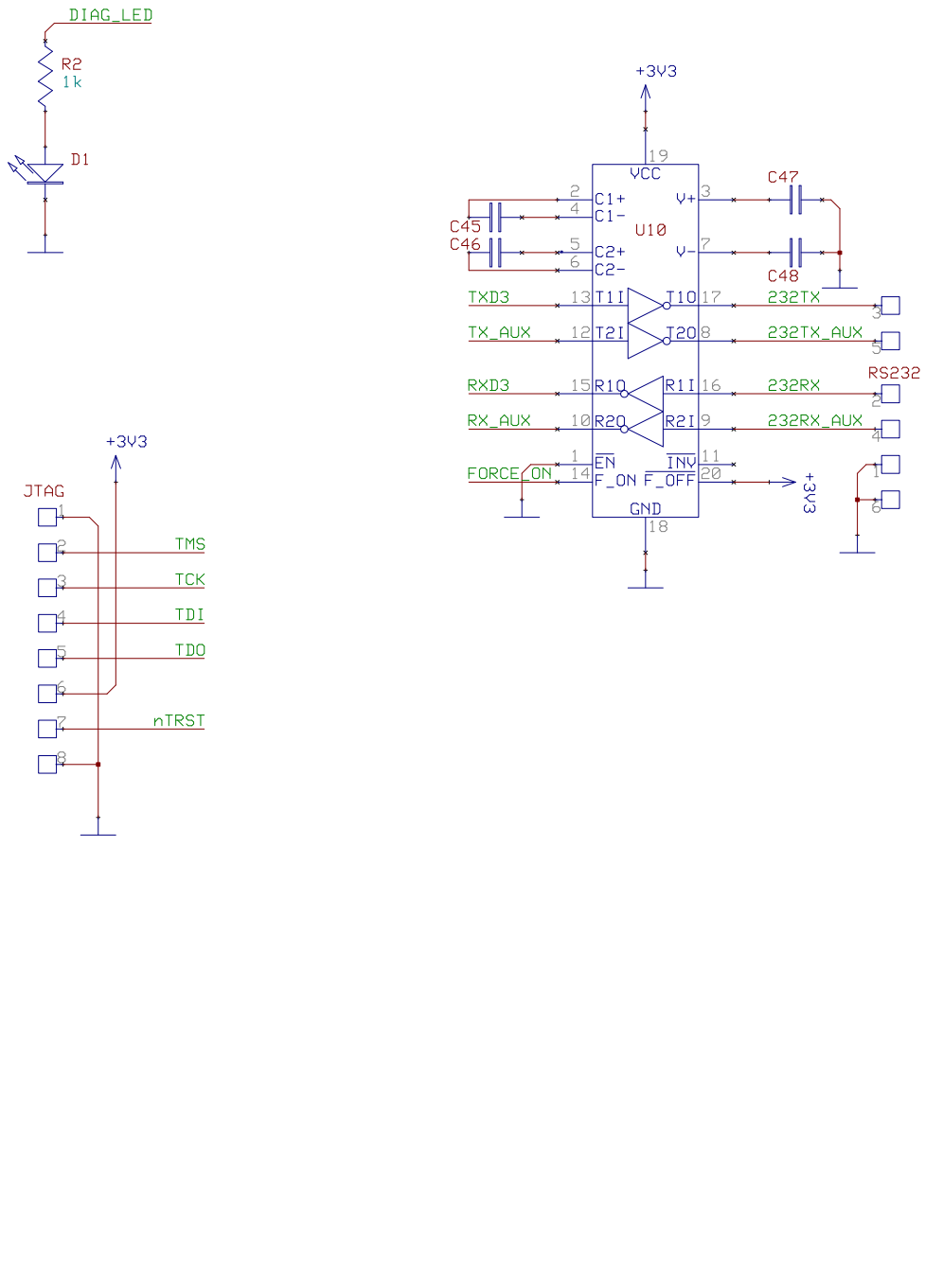
LART High speed connector
REV 4 20000429 (C)JDB



LART Low speed connector

REV 4 20000429 (C)JDB


POWER
V+
D4
30BQ040,1
C50
47u
C51
47u
R8 0R01
D2 ZHCS750,1
C49
IRF7301,2
T1
LTC1266CS,1
U11
Vin
PWR Vin
LBin
PINV
LBout
TDRIVE
SHDN
Ith
Ct
BINH
SENSE+
SENSE-
Vfb
BDRIVE
SGND
PGND
L1 22uH
R4
C54
R3
C52
C53
IRF7301,1
T1
D3
30BQ040,1
C60
R5
R9
C55
150u
C56
150u
R6 0R01
+3V3
C57
150u
D5 ZHCS750,1
C61
IRF7301,1
T2
LTC1266CS,1
U12
L2 22uH
R11
C64
R10
C62
C63
IRF7301,2
T2
D6
30BQ040,1
C65
R14
R15
R12
33k
FDV301N,1
T3
PWR_EN
C58
150u
C59
150u
R7 0R01
VCORE
EXT_RESET
RESET
C44
U9
MAX811S,1
MR
RESET
GND
VCC
nRESET
+3V3
VCORE
C1
C2
C3
C4
C5
C6
C7
C8
C9
+3V3
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
+3V3
C30
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
LART Power supply
REV 4 20000429 (C)JDB



LART Debug interfaces
REV 4 20000429 (C)JDB