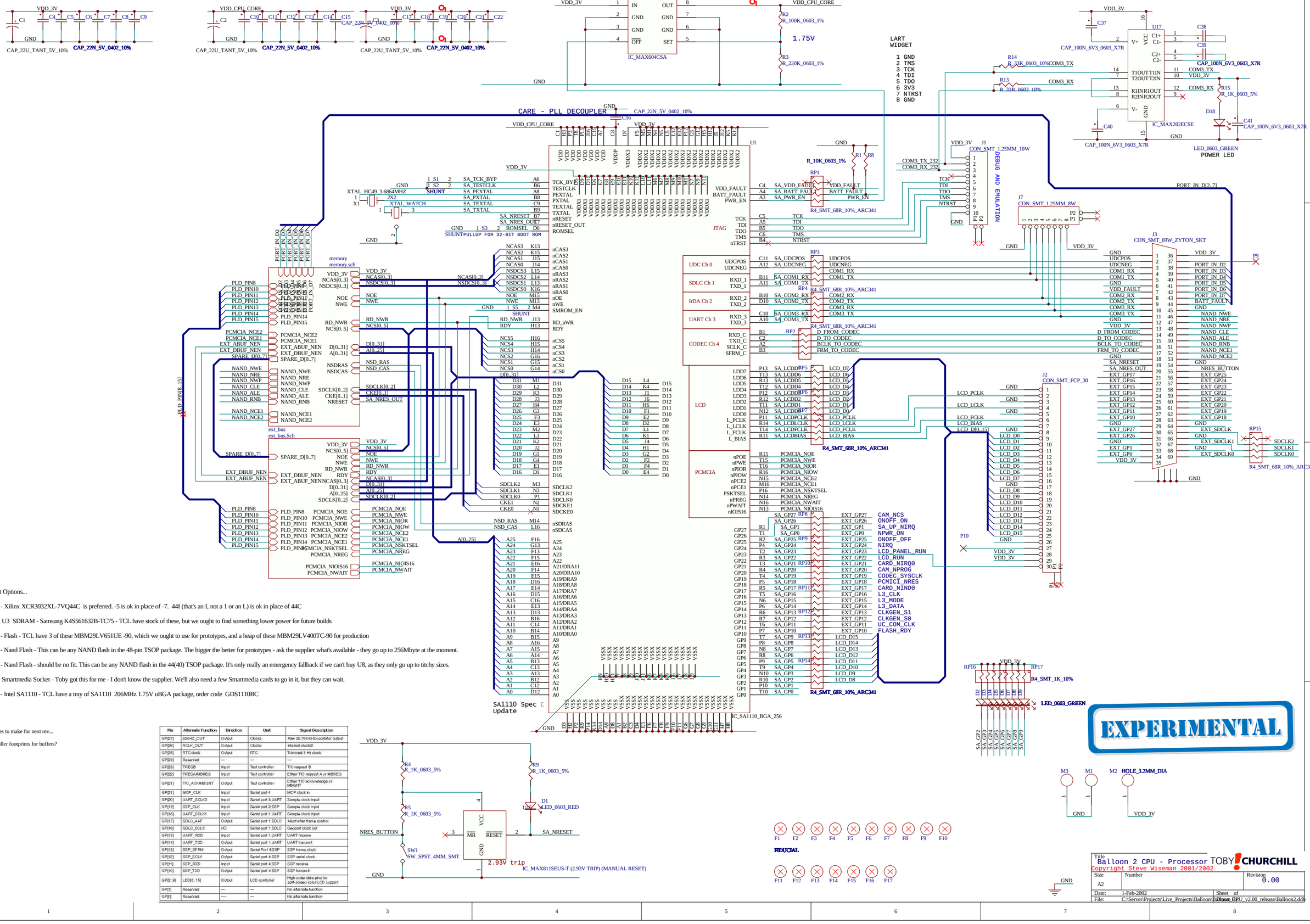


Pin	Alternate Function	Direction	Unit	Signal Description
GP[27]	32KHZ_OUT	Output	Clocks	Raw 32.768-kHz oscillator output
GP[26]	RCLK_OUT	Output	Clocks	Internal clock/2
GP[25]	RTC clock	Output	RTC	Trimmed 1-Hz clock
GP[24]	Reserved	—	—	—
GP[23]	TREQB	Input	Test controller	TIC request B
GP[22]	TREQA/MBREQ	Input	Test controller	Either TIC request A or MBREQ
GP[21]	TIC_ACK/MBGNT	Output	Test controller	Either TIC acknowledge or MBGNT
GP[21]	MCP_CLK	Input	Serial port 4	MCP clock in
GP[20]	UART_SCLK3	Input	Serial port 3 UART	Sample clock input
GP[19]	SSP_CLK	Input	Serial port 2 SSP	Sample clock input
GP[18]	UART_SCLK1	Input	Serial port 1 UART	Sample clock input
GP[17]	SDLC_AAF	Output	Serial port 1 SDLC	Abort after frame control
GP[16]	SDLC_SCLK	I/O	Serial port 1 SDLC	Geoport clock out
GP[15]	UART_RXD	Input	Serial port 1 UART	UART receive
GP[14]	UART_TXD	Output	Serial port 1 UART	UART transmit
GP[13]	SSP_SFRM	Output	Serial Port 4 SSP	SSP frame clock
GP[12]	SSP_SCLK	Output	Serial port 4 SSP	SSP serial clock
GP[11]	SSP_RXD	Input	Serial port 4 SSP	SSP receive
GP[10]	SSP_TXD	Output	Serial port 4 SSP	SSP transmit
GP[2..9]	LDD[8..16]	Output	LCD controller	High-order data pins for split-screen color LCD support
GP[1]	Reserved	—	—	No alternate function
GP[0]	Reserved	—	—	No alternate function

Title	Balloon 2 CPU - Processor TOBY CHURCHILL
Copyright	Steve Wiseman 2001/2002
Size	A2
Number	
Revision	0.00
Date:	1-Feb-2002
Sheet	of
File:	C:\Server\Projects\Live_Projects\Balloon\Balloon CPU_v2.00_release\Balloon2.ddb
Drawn By:	

SDRAM - ALWAYS

RIPPED STRAIGHT FROM ASSABET

ZERO OHM FROM 1-2

was incorrectly a 16373

VHDL

EXPERIMENTAL

LART WIDGET

1 GND
2 TMS
3 TCK
4 TDI
5 TDO
6 3V3
7 NTRST
8 GND

DEBUG AND EMULATION

ALL BLOCK 1 ON 3032

ALL BLOCK 2 ON 3032

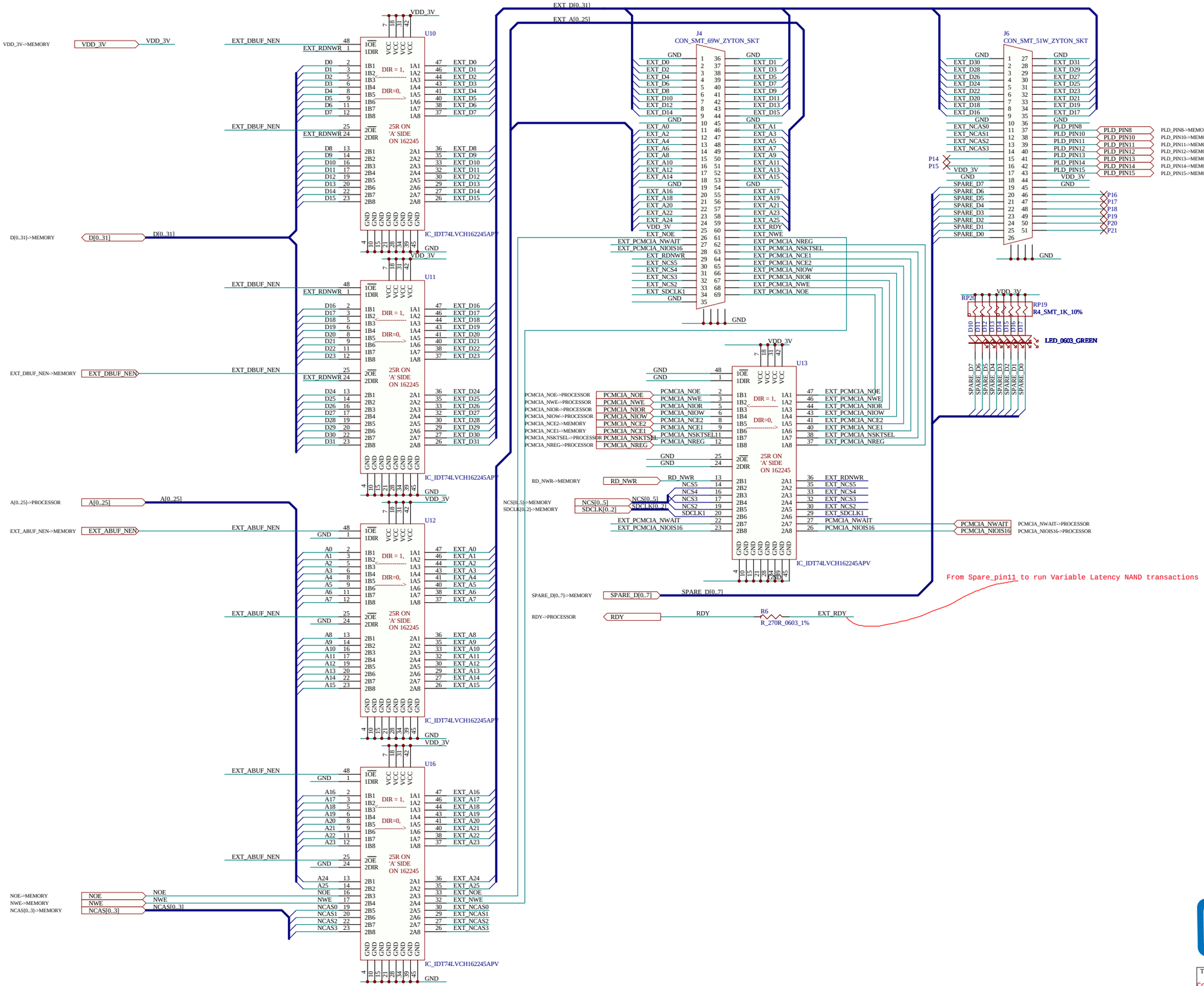
Title: Balloon 2 CPU - Memory

TOBY CHURCHILL

Size	Number	Revision
A2		0.00

Date: 1-Feb-2002 Sheet of

File: C:\Server\Projects\Live_Projects\Balloon\Balloon CPU_v2.00_release\Balloon2.ddb


EXT_D[0..31]
EXT_A[0..25]
VDD_3V
U10
U11
U12
U16
U13
IC_IDT74LVCH162245APV
25R ON
'A' SIDE
ON 162245
DIR = 1,
DIR=0,
J4
CON_SMT_69W_ZYTON_SKT
J6
CON_SMT_51W_ZYTON_SKT
VDD_3V->MEMORY
D[0..31]->MEMORY
EXT_DBUF_NEN->MEMORY
A[0..25]->PROCESSOR
EXT_ABUF_NEN->MEMORY
NOE->MEMORY
NWE->MEMORY
NCAS[0..3]->MEMORY
PCMCIA_NOE->PROCESSOR
PCMCIA_NWE->PROCESSOR
PCMCIA_NIOR->PROCESSOR
PCMCIA_NIOW->PROCESSOR
PCMCIA_NCE2->MEMORY
PCMCIA_NCE1->MEMORY
PCMCIA_NSKTSEL->PROCESSOR
PCMCIA_NREG->PROCESSOR
RD_NWR->MEMORY
NCS[0..5]->MEMORY
SDCLK[0..2]->MEMORY
SPARE_D[0..7]->MEMORY
RDY->PROCESSOR
PCMCIA_NWAIT->PROCESSOR
PCMCIA_NIOIS16->PROCESSOR
PLD_PIN8->MEMORY
PLD_PIN10->MEMORY
PLD_PIN11->MEMORY
PLD_PIN12->MEMORY
PLD_PIN13->MEMORY
PLD_PIN14->MEMORY
PLD_PIN15->MEMORY
R4_SMT_1K_10%
LED_0603_GREEN
R_270R_0603_1%
From Spare_pin11 to run Variable Latency NAND transactions
EXPERIMENTAL
Balloon 2 CPU - Exp_bus
Copyright Steve Wiseman 2001/2002
Error : toby_churchill logo.bmp file not found.
1-Feb-2002
C:\Server\Projects\Live_Projects\Balloon\Balloon BPU_v2.00_release\Balloon2.ddb