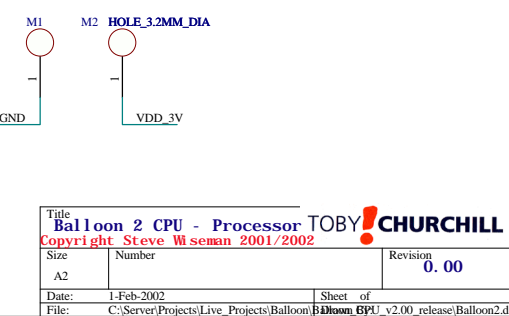
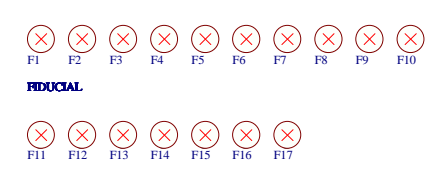
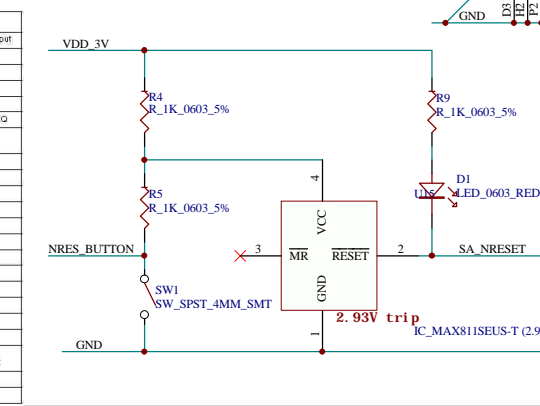


- Part Options...
- U5 - Xilinx XCR3032XL-7VQ4C is preferred. -5 is ok in place of -7. 441 (that's an I, not a 1 or an L) is ok in place of 44C
  - U2, U3 - SDRAM - Samsung K4S561632B-TC75 - TCL have stock of these, but we ought to find something lower power for future builds
  - U4 - Flash - TCL have 3 of these MBM29LV651UE-90, which we ought to use for prototypes, and a heap of these MBM29LV400TC-90 for production
  - U8 - NAND Flash - This can be any NAND flash in the 48-pin TSOP package. The bigger the better for prototypes - ask the supplier what's available - they go up to 256Mbyte at the moment.
  - U7 - NAND Flash - should be no fit. This can be any NAND flash in the 44(40) TSOP package. It's only really an emergency fallback if we can't buy U8, as they only go up to tiny sizes.
  - J8 - Smartmedia Socket - Toby got this for me - I don't know the supplier. We'll also need a few Smartmedia cards to go in it, but they can wait.
  - U1 - Intel SA1110 - TCL have a tray of SA1110 206MHz 1.75V uBGA package, order code GDS1110BC

Changes to make for next rev...

1) Smaller footprints for buffers?

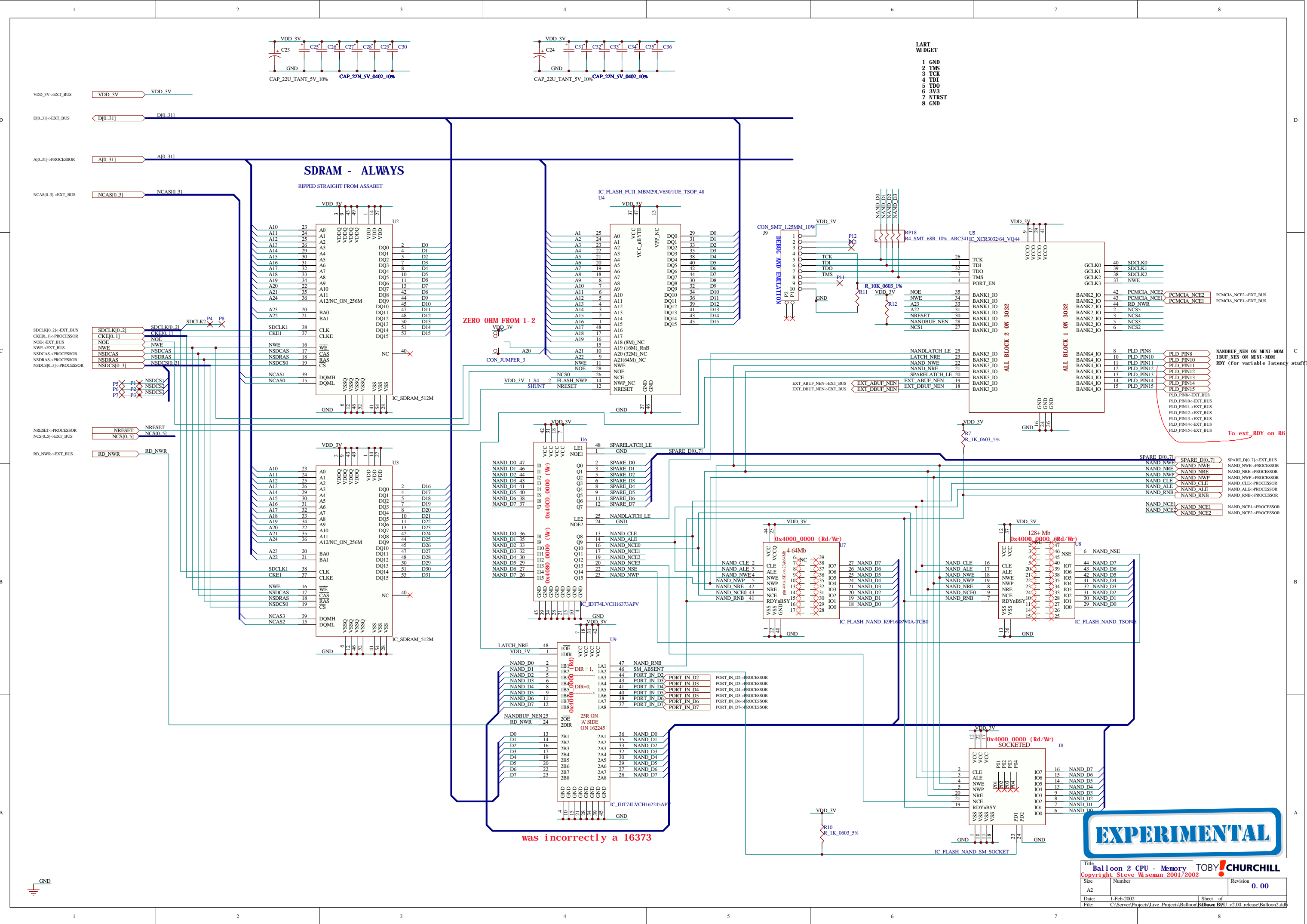
Pin	Alternate Function	Direction	Unit	Signal Description
GP27	32KHZ_OUT	Output	Clocks	Raw 32.768KHz oscillator output
GP28	RCLK_OUT	Output	Clocks	Internal clock/2
GP29	RTIC_clock	Output	RTIC	Trimmed 1Hz clock
GP30	Release	Input	—	—
GP31	TREQ0	Input	TIC controller	TIC request 0
GP32	TREQAMBREQ	Input	TIC controller	Either TIC request A or MBREQ
GP33	TIC_ACKMBGNT	Output	TIC controller	Either TIC acknowledge or MBGNT
GP34	MCP_CLK	Input	Serial port 4	MCP clock in
GP35	UART_SCLK3	Input	Serial port 3 UART	Sample clock input
GP36	SSP_CLK	Input	Serial port 2 SSP	Sample clock input
GP37	UART_SCLK1	Input	Serial port 1 UART	Sample clock input
GP38	SDCLK_AAF	Output	Serial port 1 SDCLK	Abort after frame control
GP39	SDCLK_SCLK	IO	Serial port 1 SDCLK	Output clock out
GP40	UART_RXD	Input	Serial port 1 UART	UART receive
GP41	UART_TXD	Output	Serial port 1 UART	UART transmit
GP42	SSP_SFM	Output	Serial Port 4 SSP	SSP frame clock
GP43	SSP_SCLK	Output	Serial port 4 SSP	SSP serial clock
GP44	SSP_RXD	Input	Serial port 4 SSP	SSP receive
GP45	SSP_TXD	Output	Serial port 4 SSP	SSP transmit
GP46	LED[0-16]	Output	LCD controller	High-order data pins for split-screen color LCD support
GP47	Reserved	—	—	no alternate function
GP48	Reserved	—	—	no alternate function



Title: Balloon 2 CPU - Processor TOBY  
 Copyright: Steve Weman 2001/2002  
 Size: A2  
 Date: 1-Feb-2002  
 File: C:\Server\Projects\Live Projects\Balloon 2\Balloon 2 CPU v2.00 release\Balloon2.dxp

Revision: 0.00

Sheet of: 1

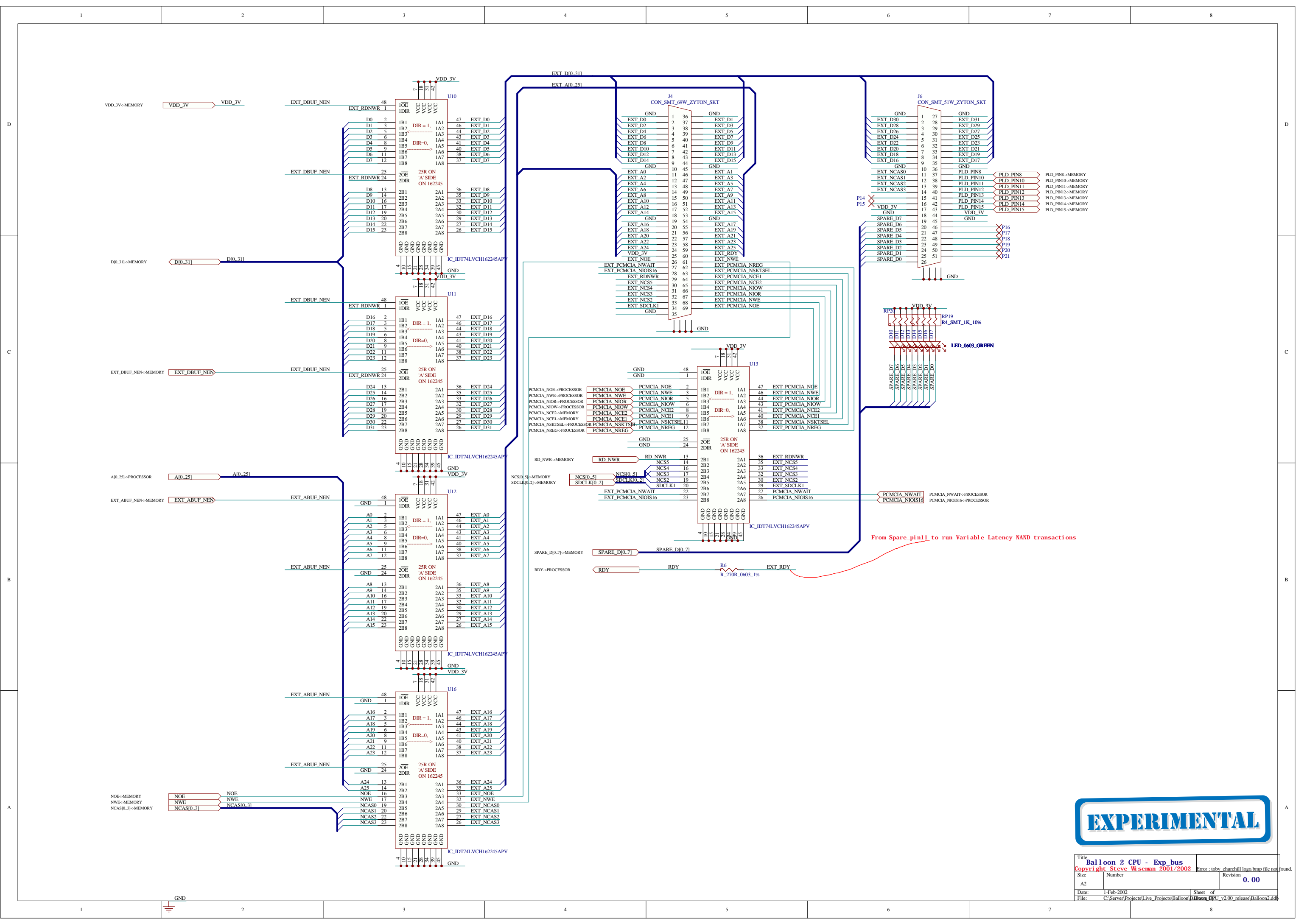


- LART WIDGET
- 1 GND
  - 2 TMS
  - 3 TCK
  - 4 TDI
  - 5 TDO
  - 6 3V3
  - 7 NTRST
  - 8 GND

ZERO OHM FROM 1-2

was incorrectly a 16373

**EXPERIMENTAL**



EXPERIMENTAL

Title		Ballroom 2 CPU - Exp_bus	
Copyright		Steve W. Seman 2001/2002	
Size	Number	Revision	0.00
Date:	1-Feb-2002	Sheet of	
File:	C:\Server\Projects\Live_P\Projects\Ballroom\Ballroom_CPU1_v2.00_release\Ballroom2.dfp		