```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
--
--  Mod history
--2002-01-08  moved flash to nCS4 rather than nCS1, to get variable latency (and an nOE per read in sequential reads)

entity balloon2 is
    Port ( noe : in std_logic;            --35
           nwe : in std_logic;            --34
           a23 : in std_logic;            --33
           a22 : in std_logic;            --31
           nreset : in std_logic;         --30
           nandbuf_nen : out std_logic;   --28
           ncs1 : in std_logic;           --27
           nandlatch_le : out std_logic;  --25
           latch_nre : out std_logic;     --23
           nand_nwe : out std_logic;      --22
           nand_nre : out std_logic;      --21
           sparelatch_le : out std_logic; --20
           ext_abuf_nen : out std_logic;  --19
            ext_dbuf_nen : out std_logic;  --18
           pld_pin8 : inout std_logic;    --8  --Now
           pld_pin10 : inout std_logic;   --10
           pld_pin11 : inout std_logic;   --11
           pld_pin12 : inout std_logic;   --12
           pld_pin13 : inout std_logic;   --13
           pld_pin14 : inout std_logic;   --14
           pld_pin15 : inout std_logic;   --15
           ncs2 : in std_logic;           --6
           ncs3 : in std_logic;           --5
           ncs4 : in std_logic;           --3
            ncs5 : in std_logic;           --2
           rd_nwr : in std_logic;         --44
           pcmcia_nce1 : in std_logic;    --43
           pcmcia_nce2 : in std_logic;    --42
           nwe_clk : in std_logic;        --37
           sdclk0 : in std_logic;         --38
           sdclk1 : in std_logic;         --39
           sdclk2 : in std_logic;         --40
           nand_d0 : in std_logic;        --26
           nand_d1 : in std_logic;        --1
           nand_d2 : in std_logic;        --32
           nand_d3 : in std_logic);       --7
end balloon2;

architecture behavioral of balloon2 is

  signal divider, last_divider, clk_enables : std_logic_vector(4 downto 0);

begin
  balloon2_process : process (sdclk1, nreset)
  begin
    if (nreset = '0') then   --do asynchronous reset stuff
        divider <= (others => '0');
        last_divider <= (others => '0');
        clk_enables  <= (others => '0');
        pld_pin8  <= '1'; -- NANDBUF_NEN on Mini-motherboard
        pld_pin10 <= '1'; -- Inbuf_nen on Mini-motherboard
        pld_pin11 <= '1'; -- RDY pin ;
    elsif (sdclk1'event and (sdclk1 = '1')) then --rising edge of sdclk2
      divider <= divider + 1;
      last_divider <= divider;
      clk_enables <= divider and not last_divider;

      pld_pin8  <= '1'; -- NANDBUF_NEN on Mini-motherboard  clk_enables(0);
      pld_pin10 <= '1'; -- Inbuf_nen on Mini-motherboard    clk_enables(1);
      pld_pin11 <= '1'; -- RDY pin  --clk_enables(2);
      pld_pin12 <= clk_enables(3);
      pld_pin13 <= clk_enables(4);
      pld_pin14 <= '0';
      pld_pin15 <= '0';

    elsif (sdclk1'event and (sdclk1 = '1')) then --rising edge of sdclk1

    end if;
  end process balloon2_process;

  --ext_dbuf_nen <= '0' when ((ncs2 = '0') or (ncs3 = '0') or (ncs4 = '0') or (ncs5 = '0')) else '1';
  --ext_abuf_nen <= '0' when ((ncs2 = '0') or (ncs3 = '0') or (ncs4 = '0') or (ncs5 = '0')) else '1';

  --nand_nre <= '0' when ((noe = '0') and (a23 = '0') and (a22 = '0') and (ncs1 = '0')) else '1';
  --nand_nwe <= '0' when ((nwe = '0') and (a23 = '0') and (a22 = '0') and (ncs1 = '0')) else '1';

  --nandlatch_le  <= '1' when ((noe = '0') and (a23 = '1') and (a22 = '0') and (ncs1 = '0')) else '0';
  --sparelatch_le <= '1' when ((nwe = '0') and (a23 = '1') and (a22 = '1') and (ncs1 = '0')) else '0';

  --latch_nre <= '0' when ((noe = '0') and (a23 = '0') and (a22 = '1') and (ncs1 = '0')) else '0';

  --nandbuf_nen <= '0' when (ncs1 = '0') else '1';


  ext_dbuf_nen <= '0' when (((ncs2 = '0') or (ncs3 = '0') or (ncs4 = '0') or (ncs1 = '0')) and (rd_nwr = '0')) else '1';  --note that we can't mirror r
                                                                                                                        --direction controlled from a
  ext_abuf_nen <= '0' when ((ncs2 = '0') or (ncs3 = '0') or (ncs4 = '0') or (ncs1 = '0')) else '1';

  nand_nre <= '0' when ((noe = '0') and (a23 = '0') and (a22 = '0') and (ncs4 = '0')) else '1';
  nand_nwe <= '0' when ((nwe = '0') and (a23 = '0') and (a22 = '0') and (ncs4 = '0')) else '1';

  nandlatch_le  <= '1' when ((nwe = '0') and (a23 = '1') and (a22 = '0') and (ncs4 = '0')) else '0';
  sparelatch_le <= '1' when ((nwe = '0') and (a23 = '1') and (a22 = '1') and (ncs4 = '0')) else '0';

  latch_nre <= '0' when ((noe = '0') and (a23 = '0') and (a22 = '1') and (ncs4 = '0')) else '1';

  nandbuf_nen <= '0' when (ncs4 = '0') else '1';

end behavioral;
```